Amendments to the Specification:

Please replace paragraph on Pg. 4, Lines 7-10 with the following amended paragraph:

Figure 1B shows the parallel termination case wherein the terminated resistor [[R_{TERM}]]Z_{TERM} is selected to have an impedance value which is equivalent to the impedance of the transmission line Z_L in order to prevent signal reflection back to the transmitter. These terminations are conventional.

Please replace the paragraph beginning at Pg. 4, Lines 11 with the following amended paragraph:

At high operating frequencies, it cannot be assumed that the input of the receiver R is an open circuit into the presence of an input parasitic capacitor in order to be able to treat the receiver R as an open circuit, thus the signal applied to the input of the receiver R will charge/discharge the parasitic capacitor. Such charging/discharging means that the signal that is received by the receiver R will be distorted. The same situation occurs with the parallel termination shown in Figure 1B wherein the terminating resistor [[R_{TERM}]]Z_{TERM} is in parallel with the parasitic capacitance C_P. In addition, the higher the frequency, the greater the distortion. This distortion is particularly referred to as a "glitch" when the receiver has to have a strong signal and a spike is heard as a result of the distortion.

Please replace the paragraph beginning at Pg. 5, Line 21 with the following amended paragraph:

With reference to Figure 2C, the input signal is shown applied to the I/O pad P through the transmission line represented by the impedance Z_L. The tracking

system employs a capacitor C_T having one terminal coupled to one terminal of the parasitic capacitance C_P and the other terminal coupled between a current source 12 and an NMOS transistor 14 having its gate coupled its drain, as well as with the gate of the second NMOS transistor 16. A PMOS transistor 18 has its drain and gate coupled to a drain of NMOS transistor 16 as well as with the gate of the second PMOS transistor 20.

Please replace the paragraph beginning at Pg. 5, Line 28 with the following amended paragraph:

In operation, during a rising edge signal (+dv/dt), since the voltage of C_T cannot change instantaneously, the voltage increases at terminal 22 which ultimately causes the drain of PMOS transistor 20 to provide sufficient current at terminal 24 to compensate for a portion of the current that would otherwise be provided to parasitic capacitance C_P by the input signal.